AMENDMENTS TO THE CLAIMS

IN THE CLAIMS:

A complete set of claims is provided below.

1. (Canceled)

2. (Canceled)

3. (Currently Amended) ~~**The apparatus of Claim 1**~~ **An apparatus comprising:**

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-down network wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network, wherein said differential pull down network comprises an enhanced special differential pull down network that uses dummy transistors to form a pass-gate which is closed during evaluation for a differential input.

4. (Currently Amended) ~~**The apparatus of Claim 1**~~ **An apparatus comprising:**

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-down network wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network, wherein said differential pull down network comprises an enhanced special differential pull down network that uses dummy transistors to form a pass-gate which is always closed, said pass gate inserted if different discharge paths have unequal numbers of transistors.

5.-11. (Canceled)

12. (Currently Amended) ~~**The apparatus of Claim 1**~~ **An apparatus comprising:**

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-down network wherein, for a stable input combination,

internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network, wherein said differential pull up network comprises an enhanced special differential pull up network that uses dummy transistors to form a pass-gate which is closed during evaluation for a differential input.

13. (Currently Amended) ~~**The apparatus of Claim 1**~~ **An apparatus comprising:**

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-down network wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network, wherein said differential pull up network comprises an enhanced special differential pull up network that uses dummy transistors to form a pass-gate which is always closed, said pass gate inserted if different discharge paths have unequal numbers of transistors.

14.-25. (Canceled)